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Application No. 10/035,587
Attorney Docket No. 06502.0369-00

PATENT
Customer No. 22,852

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Guy L. STEELE, Jr.	)	Group Art Unit: 2193
	)	
Application No.: 10/035,587	)	Examiner: Mai, Tan V.
	)	
Filed: December 28, 2001	)	
	)	
For: FLOATING POINT STATUS INFORMATION ACCUMULATION CIRCUIT	)	Confirmation No.: 2874
	)	

Attention: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY BRIEF

Pursuant to the provisions of 37 C.F.R. § 41.41 and M.P.E.P. § 1207.03(V), Appellant requests that this appeal be maintained, for the reasons set forth in this Reply Brief, filed in response to the Examiner's Answer mailed December 27, 2006. This Reply Brief is being timely filed within two months of the Examiner's Answer.

If any fees are required, Appellant requests that the required fees be charged to Deposit Account No. 06-0916.

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I. STATUS OF CLAIMS

Claims 1-47 remain pending and under current examination. Claims 1-3 and 5-47 are subject to this appeal.[1]

[1] Claim 4 is objected to as allowable if rewritten in independent form.

II. GROUNDS OF REJECTION TO BE REVIEWED

A. Claims 1-3 and 5-47 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,995,991 to Huang et al. ("Huang").

B. Claims 1-3 and 5-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,009,511 to Lynch et al. ("Lynch").

III. ARGUMENT

This Reply Brief supplements the Appeal Brief filed April 7, 2006 by responding to the Examiner's Answer mailed December 27, 2006 that included new grounds of rejection. This Reply Brief responds to the Examiner's new arguments, where appropriate, and to the new rejections in the Examiner's Answer.

A. The new rejection of claims 1-3 and 5-47 under 35 U.S.C. § 102(b) as being anticipated by Huang

The rejection of claims 1-3 and 5-47 under § 102 as anticipated by Huang is incorrect for the same reasons set forth in Appellant's appeal brief in response to the previous rejection of claims 1-3 and 5-47 under § 103 based on Huang, in which Appellants specifically pointed out the elements of claims 1-3 and 5-47 which are not taught by Huang.

With respect to claim 1, as best understood by Appellant, the Examiner alleges that Huang's X register 116 (Fig. 4) constitutes the claimed "operand" and that Huang's X_tag 116-2 constitutes the claimed "status flag information." Examiner's Answer at 13-14. These allegations are incorrect. Stated simply, a register is not an "operand," as recited by claim 1. A register is hardware—a device that stores information. In contrast, an operand is a quantity on which a mathematical operation is performed. Therefore, Huang's register 116 does not constitute the claimed "operand."

Moreover, Huang's operand portion 116-1 does not constitute the claimed "operand." As clearly illustrated in Fig. 4 of Huang, the x_tag 116-2 (alleged status flag information) is separate from operand portion 116-1, not "encoded" within the operand portion, as recited by claim 1.

Furthermore, the Examiner's allegations regarding claims 1-3 and 5-47 are not clear. The Examiner states "Although the tag generator (150) [of Huang] to generate the tag value separately from the output of arithmetic section (114), the examiner believes that the resulting status 'tag value' embedded within the 'resulting floating point operand'. It is noted that the format [resulting status embedded within the resulting floating point operand data] of **stored data** in the MEMORY (REGISTER FILE) 112 is the **same as** the format [status data within the floating point operand] of **data transferred** to 'X' or 'Y' register because the **read out / write in data** is usually unchanged. Therefore, the **stored** 'resulting floating point operand' includes the 'resulting status' as claimed." Examiner's Answer at 14 (emphasis in original). These new allegations cannot be understood. The Examiner concedes that the tag value of Huang is generated separately from the operand. Id. The Examiner's "belief" does not cure this concession nor does it constitute a teaching or suggestion by Huang of each and every element recited by claim 1.

Because the Examiner generally references Huang's tag generator 150, Appellant points out that, contrary to the claimed structure, tag generator 150 of Huang generates the tag (alleged status flag information) separately from the operand generator 122, and that the tag value is stored separately in x_tag 116-2 from operand portion 116-1. As noted above, the Examiner concedes this. Examiner's Answer at 14. Therefore, Huang's Fig. 4 illustrates that the "status flag information" is not "encoded" within the "operand," as recited by claim 1, either at generation or during storage.

Claim 2 is allowable at least because it depends from allowable claim 1.

In the Examiner's Answer, the Examiner rejects claim 3 by asserting: "the claim adds 'further comprising one or more **operand buffers**. The memory (register file) 112 in Huang's Fig. 4 corresponds to the claimed 'operand buffer' . . . . ." Examiner's Answer at 5 (emphasis in original). Even assuming Huang's register file 112 could be an operand buffer, the Examiner has not addressed how Huang allegedly transfers the operands in the alleged operand buffer "to the analysis circuit," or even how Huang could teach or suggest an "analyzer circuit," as recited by claim 3.

The Examiner summarily rejects claims 5-17, stating that "the claims add the detail 'formats', 'flags', 'status," and then stating that "[t]hese features are inherent in special floating point number disclosed in Huang." Examiner's Answer at 5. In responding to reasoning in Appellant's Appeal Brief, the Examiner further alleges: "Huang does teach claimed 'status' information, e.g., zero, overflow, underflow, etc. status flags (col. 7, lines 20-23); Not a number, etc. (TABLE 1). Also, Huang' s [sic] claim 3 discloses 'positive infinity' & 'negative infinity' features as Appellant's claim 14." Examiner's Answer at 14. The Examiner thus appears to assert that that the elements in claims 5-17 are inherent in Huang.

M.P.E.P. § 2112 instructs: "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic" (emphasis in original). Rather, "the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Id. (emphasis in original). The Examiner has not provided any basis in fact or technical reasoning to support his general allegation that the claimed elements are

inherent in the disclosure Huang. Accordingly, the Examiner's reliance on inherency is improper and the rejection of claims 5-17 should be withdrawn.

Moreover, Huang does not teach or suggest, for example, "a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format," as recited by claim 5 (emphasis added); "an invalid operation flag, an overflow flag, an underflow flag, a division by zero flag, and an inexact flag," as recited by claim 6 (emphasis added); an "overflow format [that] represents one of a +OV status and a –OV status", as recited by claim 7; an "overflow format [that] includes a set inexact status flag," as recited by claim 8; an "underflow status [that] represents one of a +UV status and a – UV status," as recited by claim 9; an "underflow format [that] includes a set inexact status flag," as recited by claim 10; a "least significant bit in the plurality of operands [that] represents a set inexact status flag," as recited by claim 11; "one of a commutative and an associative flag-combining operation," as recited by claim 12; "a sign bit in the accumulated result [that] is a logical OR of sign bits in the plurality of operands," as recited by claim 16; or producing "the accumulated result in a NaN formatted one of the plurality of operands," as recited by claim 17.

Independent claims 18 and 33, although of different scope than claim 1, patentably distinguish from Huang for at least the same reasons as claim 1. Claims 19-32 and 34-47 depend from independent claims 18 and 33 and therefore include all of the elements recited therein. Dependent claims 19-32 and 34-47 are also allowable for the same reasons discussed above with respect to claims 2, 3, and 5-17. Accordingly,

Huang cannot anticipate claims 1-3 and 5-47. Appellant requests the Board to overturn the rejection of claims 1-3 and 5-47.

B. The rejection of claims 1-3 and 5-47 under 35 U.S.C. § 103(a) as being unpatentable over Lynch

In the Examiner's Answer, the Examiner alleges: "the examiner interprets the floating point register [stack] as a operand." Examiner's Answer at 15. As discussed above, (1) a hardware register stack is not an operand; (2) Lynch does not teach or suggest the claimed "operands each of which ha[s] encoded status flag information," and (3) Lynch suffers from the same drawbacks of the prior art discussed in Appellant's specification. Independent claims 18 and 33, although of different scope than claim 1, patentably distinguish from Lynch for at least the same reasons as claim 1.

In the Examiner's Answer, the Examiner has failed to address each and every element recited by claims 3, 5-17, 20-32, and 35-47. The Examiner merely alleges: "Lynch teaches the claimed 'status' information, e.g., '[t]ypes of special floating point numbers include zero, +infinity, -infinity, and NaNs' (col. 17, lines 6-7) and Fig. 5. In col. 18, first complete paragraph, Lynch discloses '+infinity' & '-infinity' features as Appellant's claim 14." Examiner's Answer at 15 (emphasis added).

The Examiner provides no explanation of how Lynch allegedly teaches or suggests:

(1) "a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format," as recited by claim 5 (emphasis added);

(2) "an invalid operation flag, an overflow flag, an underflow flag, a division by zero flag, and an inexact flag," as recited by claim 6 (emphasis added);

(3) an "overflow format [that] represents one of a +OV status and a –OV status", as recited by claim 7;

(4) an "overflow format [that] includes a set inexact status flag," as recited by claim 8;

(5) an "underflow status [that] represents one of a +UV status and a – UV status," as recited by claim 9;

(6) an "underflow format [that] includes a set inexact status flag," as recited by claim 10;

(7) a "least significant bit in the plurality of operands [that] represents a set inexact status flag," as recited by claim 11;

(8) "one of a commutative and an associative flag-combining operation," as recited by claim 12;

(9) "a sign bit in the accumulated result [that] is a logical OR of sign bits in the plurality of operands," as recited by claim 16; or

(10) producing "the accumulated result in a NaN formatted one of the plurality of operands," as recited by claim 17.

The Examiner's allegations that these elements are "inherent" and "well known" do not cure these deficiencies. See Examiner's Answer at 7-8. Appellant's claim 14 does not recite "+ infinity" & "-infinity", as asserted by the Examiner, demonstrating the Examiner's failure to carefully address each and every element recited by the claims. Finally, the Examiner still has not provided any basis for rejecting claims 15 and 16. Id.

IV. CONCLUSION

The additional reasons given above supplement, in response to the Examiner's Answer, those presented in the Appeal Brief filed on April 7, 2006 and demonstrate that pending claims 1-47 are allowable. Appellant respectfully requests that the Board reverse the Examiner's rejections.

If any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Reply Brief, Appellant requests such an extension. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 that are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 20, 2007

By: _____
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